What is claimed is:

1. A clock switching circuit for receiving as an input a plurality of clock signals including a first and second clock signals and switching one clock signal to be output from said first clock signal to said second clock signal, comprising:

a plurality of unit circuits for respectively receiving as an input said clock signals, selection signals of the clock signals and enabling signals and controlling supplying and stopping of said clock signals in accordance with said selection signals and said enabling signals; and

a feedback circuit for monitoring output conditions of said plurality of unit circuits and, when outputting of all clock signals of said plurality of unit circuits was stopped as a result of stopping said first clock signal, giving a plurality of said unit circuits said enabling signals for approving starting of a supply of said second clock signal.

2. A clock switching circuit as set forth in claim 1, wherein each of said plurality of unit circuits comprises a delay unit for delaying timing of changing a voltage level indicating a supplying condition of said first clock signal to a voltage level indicating a

stopping condition of a monitor signal used for monitoring said output condition when an instruction of stopping said first clock signal is given by said selection signal, and delaying an operation of starting a supply of the second clock signal by using a point that said enabling signal becomes active as a starting point when an instruction of starting a supply of said second clock signal is given by said selection signal.

3. A clock switching circuit as set forth in claim 1, wherein:

each of said plurality of unit circuits further comprises a clock output gate unit, whose operation timing is controlled by said delay unit, for stopping or starting outputting of input said clock signal; and

said delay unit and said clock output gate unit operate in synchronization with said input clock signal.

4. A clock switching circuit as set forth in claim 1, further comprising:

an output circuit at a final stage connected to all outputs of said plurality of unit circuits for outputting any one of said plurality of clock signals output from said plurality of unit circuits; and

a plurality of synchronization portions provided at an input stage for said selection signal in each of said plurality of unit circuits for operating in synchronization with a clock signal output from said output circuit to unify phases of said selection signals of said plurality of unit circuits.

5. A clock switching circuit as set forth in claim 1, wherein:

said delay unit operates in synchronization with said input clock signal, and further comprising

a synchronization portion provided at an input stage of said delay unit in each of said plurality of unit circuits for operating in synchronizing with said input clock signal.

6. A clock switching circuit as set forth in claim 1, further comprising:

an output circuit at a final stage connected to all outputs of said plurality of unit circuits for outputting any one of said plurality of clock signals output from said plurality of unit circuits; and

wherein said output circuit at the final stage comprises a discharge portion for discharging an output side node of the output circuit in accordance with

said enabling signal.